Name:_____ **Student Number:**_____

1) a) For the circuit shown in Figure 1 draw the DC load line and indicate the Q point on this line.
(Use the supplied transistor curve and label the X and Y axis' values)

b) Also determine the ac voltage gain (Av) of this transistor amplifier? Av = _____

c) Is this a stiff voltage divider bias circuit? **(Show work no guessing is allowed!)**

Yes ☐ No ☐

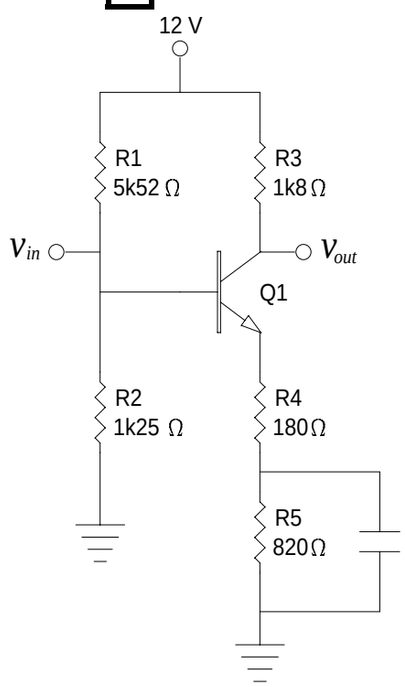
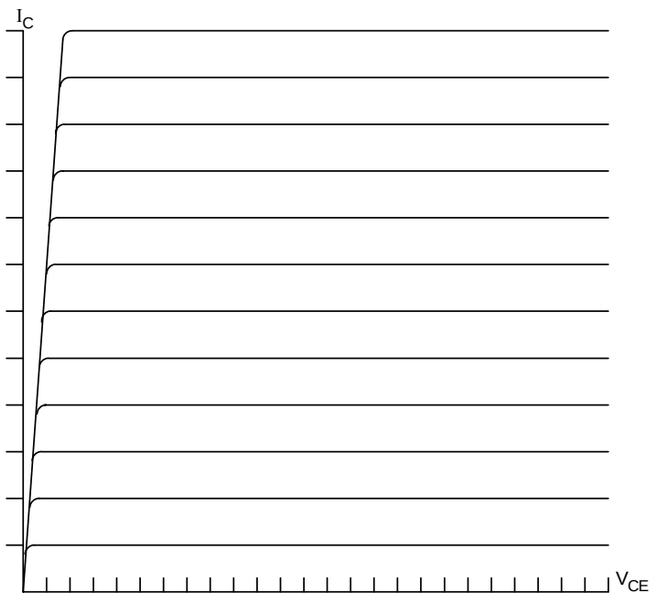


Figure 1

I_{CQ} = _____ V_{CEQ} = _____



Name:_____ **Student Number:**_____

Name:_____ **Student Number:**_____

2) For the circuit shown in Figure 2, Q1 and Q2 have identical electrical characteristics:

$V_{BE} = 0.7$ V, $\beta = 100$, $I_{CBO} = 0$.

Also you may assume that $I_C = I_E$ for this circuit.

Find the Tail current (I_{Tail}), the voltage from terminal A to ground (V_A) the voltage from terminal A to terminal B (V_{AB}) as well as the differential gain (A_{dm}).

I_{Tail} = _____

V_A = _____ V_{AB} = _____

A_{dm} = _____

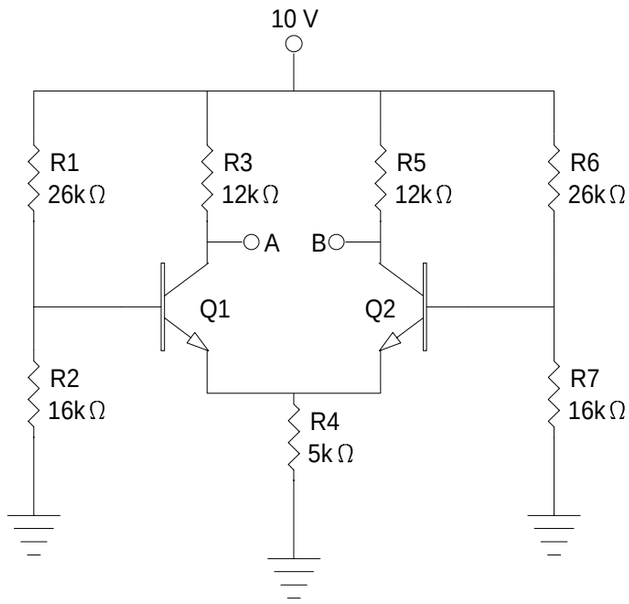


Figure 2

Name:_____ **Student Number:**_____

Name:_____ **Student Number:**_____

3) a) For the two stage amplifier shown in Figure 3, calculate the input impedance, Zin, output impedance, Zout, and the overall voltage gain $A_{V(Total)}$.

Assume $\beta = 100$, $|V_{BE}| = 0.7V$, $V_{CE(sat)} = 0.3$ V, $I_{CBO} = 0$, and that the amplifiers are biased properly.

Zin = _____ Zout = _____ $A_{V(Total)}$ = _____

b) What would the output voltage be in volts peak to peak if the input generator had a source resistance of 1k816 Ω and a level of 10 mV_{RMS} and the amplifier was driving an external 23 kΩ load?

v_{out} = _____ V_{P-P}

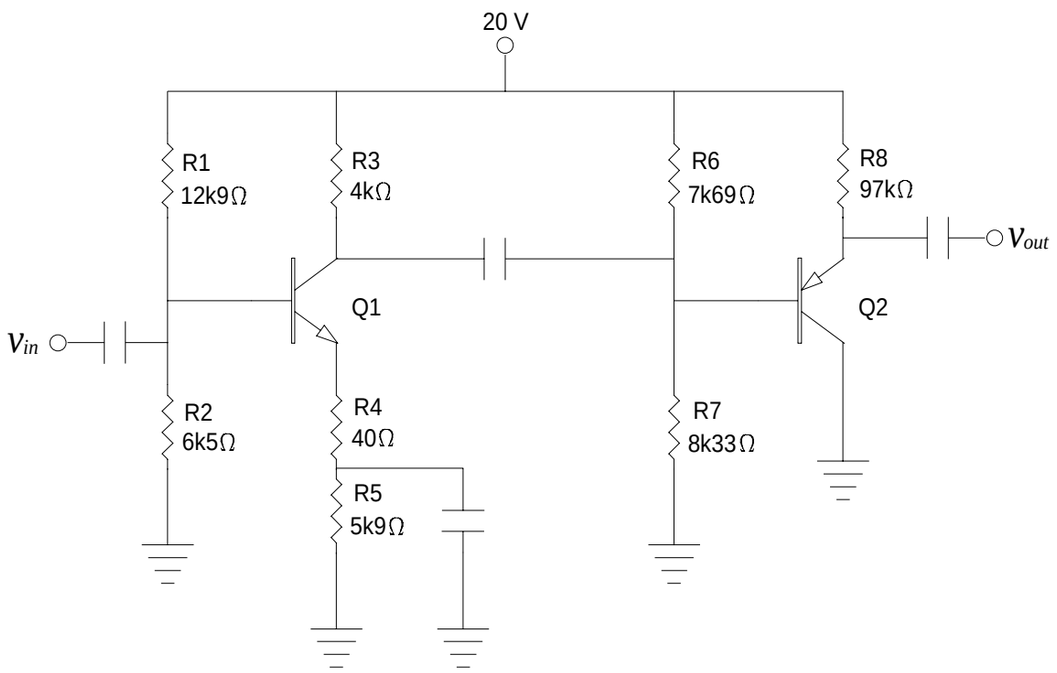


Figure 3

Name:_____ **Student Number:**_____

Name:_____ **Student Number:**_____

4) a) Using the diagram shown in Figure 4, design a JFET common source amplifier that has the following specifications:

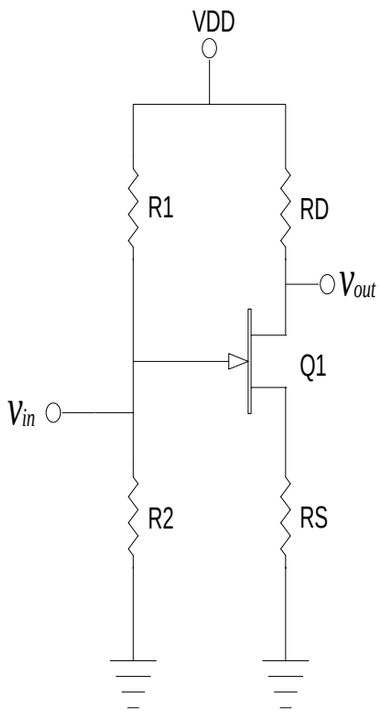
V_{DD} = 30 V, $Zin_{(Min)}$ = 1M Ω, Zout = 4k5 Ω, |Av| = 20, $Zin_{(Max)}$ = 1M1 Ω.

R1 = _____ R2 = _____

RD = _____ RS = _____

b) With RD = RS, what voltage level would V_{DD} need to be if we want V_{DSQ} to be in the middle of the V_{DS} load line?

V_{DD} = _____



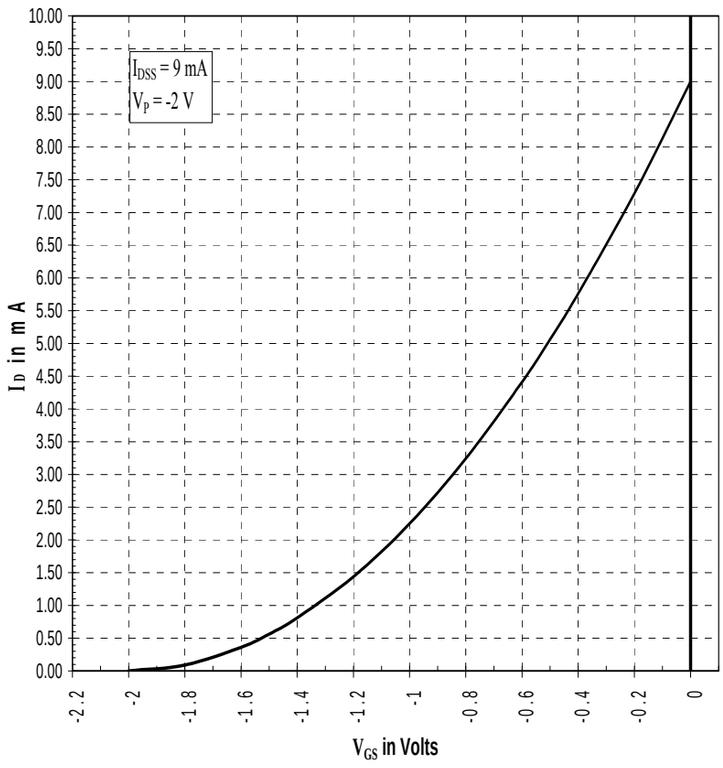


Figure 4

Name:_____ **Student Number:**_____

Name:_____ **Student Number:**_____

5) For the circuit shown in Figure 5, Q1 and Q2 are matched transistors and therefore have identical electrical characteristics:

V_{BE} = 0.7 V, $V_{CE(Sat)}$ = 0.3 V, β = 100, I_{CBO} = 0 as well $I_{B1} = I_{B2}$.

Determine the voltage across (VLoad) and the current through (ILoad) if RLoad is 10 kΩ and 40 kΩ.

RLoad	10 kΩ	40 kΩ
VLoad		
ILoad		

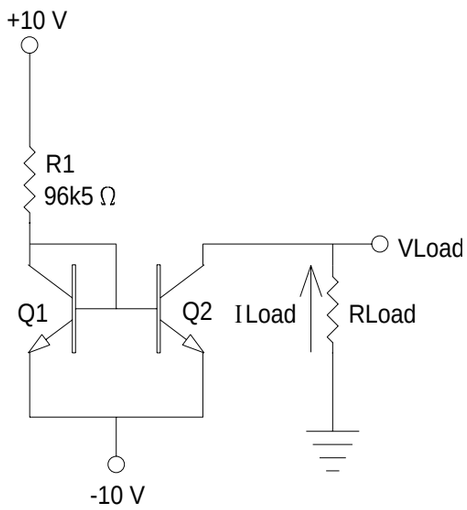


Figure 5

Name:_____ **Student Number:**_____